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Abasement of Harmonics by Adopting Fault-tolerant Nine-level Inverter for Grid- independent PV System

P. Venkatachalam[1], K. Dileep Kumar Reddy[2]

Dept. of Electrical and Electrical Engineering, JNTUACEP, Pulivendula, A.P, India[1]

Lecturer, Dept of EEE, JNTUACEP, Pulivendula, A.P, India[2]

Abstract: In this paper, a fault-tolerant single-phase nine-level inverter configuration is proposed for photo-voltaic (PV) generation systems. Conventional two-level inverters are popularly used in PV applications, but these inverters provide the output voltage with considerable harmonic content. One of the efficient ways to improve the power quality of PV generation systems is to replace a two-level inverter with a multilevel inverter. Conventional multilevel inverters reduce total harmonic distortion and filter requirements effectively, but it has limitations in terms of reliability due to increased device count and capacitor voltage balancing issues. Therefore, a fault-tolerant single-phase five-level inverter is presented, which is constructed by using a half-bridge two-level inverter, a three-level diode clamp inverter, and a bidirectional switch. fault-tolerant single-phase five-level inverter has less number of switching devices compared to conventional five-level inverters, but these inverter also provides considerable harmonic content. Therefore a fault-tolerant single-phase nine-level inverter is presented. The proposed inverter topology can tolerate the system faults due to failure of the source and/or switching devices with least modification in the switching combinations. Nine-level inverter configuration is formed by cascading the two five-level inverters. The proposed system under normal and faulty condition is simulated in MATLAB/Simulink environment.

Keywords: Fault-tolerant multilevel inverters, photo-voltaic (PV) generation system, power quality, total harmonic distortion (THD).

I. INTRODUCTION

Renewable energy sources such as solar and wind energy systems are gaining more attention both in re-search and industry communities to reduce the dependence on conventional fossil fuel systems [1]. In particular, the continuous improvement in semiconductor technology for solar cell fabrication increases the cell efficiency and hence motivates the use of photovoltaic (PV) systems widely [2].Conventional multilevel inverters are introduced in [7] and [8], which reduce filter size requirement and improve power quality of PV generation systems by reducing total harmonic distortion. However, these multilevel inverters offer limitations in terms of more number of power device requirement for a given number of voltage levels [9], capacitor voltage balancing problems, and reliability issues. By addressing some of the aforementioned issues, many multilevel inverter topologies are presented in literature with reduced number of devices for PV generation systems and drive applications [10]–[14].

In these topologies, although the switch count is reduced, any one of the switch or source failure may lead to overall system shutdown.

The off-grid PV generation system is a preferable choice for electrification option for geographically remote areas and islands which are far from the grid [15]. The faults in these systems such as source and switch failure may cause overall system shut down and take longer time to recover. These issues bring in the need of fault-tolerant converters for PV generation systems to provide continuous power to essential loads. In this regard, switch failure issues of multilevel inverters are addressed in [16] without compromising on the number of levels even under fault condition. In [17], a fault - tolerant topology for grid-connected PV application using a coupled Scott transformer is proposed. In normal condition, the topology operates with less number of switches, but during fault, it requires an additional leg to replace the faulty switch. The survey of fault-tolerant techniques for three-phase two-level and multilevel inverters is discussed in [18]. Also, it has clearly discussed the importance and need for continuous development of fault-tolerant multilevel inverters. The paper presents an open-circuit fault-tolerant control strategy for a T-type Five-level inverter without using additional switches. The previously discussed topologies with single or multiple sources have no fault tolerance capability with respect to source failure and energy-sharing capability.

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To address the previously discussed issues in this paper, a single-phase Nine-level inverter topology is proposed for PV applications. The proposed topology has fault-tolerant capability in case of any one of the source and/or switch open fault. The accomplishment of fault tolerance with least changes in switching pattern and less number of active switches makes the topology more reliable.

Power converter plays an important role for conversion of renewable source energy to standardized form of energy. Therefore, efficient design of power converter is needed to ensure good power quality and reliability. The dc output of the renewable energy sources like solar energy is converted into ac in a two stage process. The first stage is to boost the low output voltage of the PV array and to extract maximum power from it using a suitable MPPT technique, with the help of a dc to dc converter [3]. Second stage is for converting the boosted dc to ac using a dc to ac converter. Generally, the two stage process uses a two level inverter which will introduce considerable harmonic content along with the fundamental voltage [4]. These harmonics increases loss in the system causing total generation system efficiency to decrease. To increase the efficiency of the total solar system the two stage conversion process is reduced to a single stage process using three phase boost inverter [5] with SVPWM, but here also relatively the harmonics in the output voltage is high. Diode clamped, cascade h-bridge multilevel inverter fed with multiple PV strings and MPPT control of individual PV strings improves the efficiency of the system. In these inverters the stability control of PV generation system is discussed for different irradiation, temperature changes and mismatch of PV strings. Many multilevel inverters topologies are discussed for renewable energy applications with reduced number of semiconductor devices. These multilevel inverters use, equal ratings of voltage sources to supply energy to load. However, the equivalent loading of each sources over a complete fundamental cycle are quite different which leads to underutilization of voltage sources.

II. PROPOSED NINE LEVEL INVERTER CONFIGURATION

The block diagram of the proposed fault tolerant single phase Nine-level inverter circuit is shown in fig.1 The proposed nine-level inverter configuration is formed by cascading the two five-level inverters, in which each five-level inverter is realized by connecting a three-level neutral-point-clamped inverter to one side of the load, and the other side of the load is connected with a two-level half-bridge inverter depicted in fig.1 The bidirectional switches S5, S15 are connected between the neutral point of two sources and the single leg of the half-bridge inverter. For better understanding, the topology is supplied by two equal dc links Vdc1, Vdc2, Vdc3 and Vdc4, respectively. All sources are equal i.e., Vdc1=Vdc2=Vdc3=Vdc4 =Vdc. It is known that top five-level inverter is capable of generating voltage levels of Vdc, 2Vdc, 0, and – Vdc, -2Vdc; similarly, the bottom five-level inverter can generate two voltage levels with magnitudes of Vdc, 2Vdc, 0, and – Vdc, -2Vdc. As a result, in combining both, the total effective voltage across the load will have a total of nine voltage levels with magnitudes of 4Vdc, 3Vdc, 2Vdc, Vdc, 0, and – Vdc, -2Vdc, –3Vdc, -4Vdc.

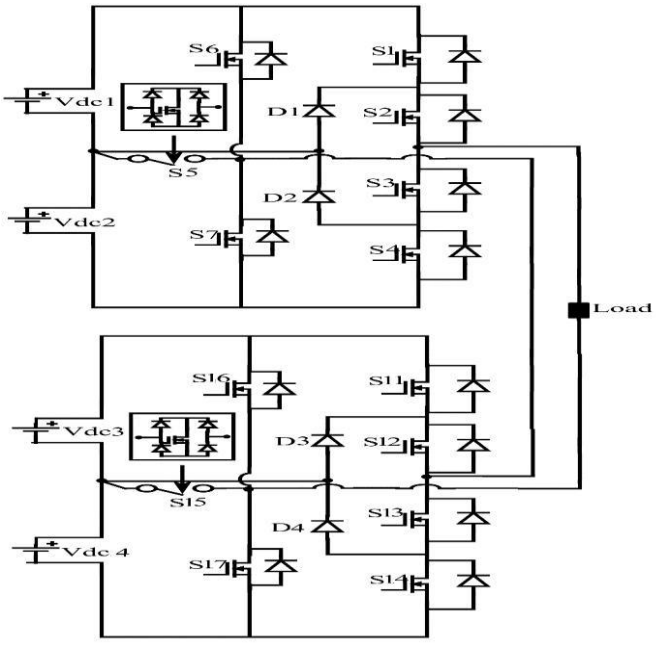

Fig.1 proposed fault-tolerant nine-level inverter

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The switching combination for five-level voltage generation and direction of current during each voltage level is given in Table-1. The switches S5, S15 provides switching redundancy for voltage levels Vdc, 0, and − Vdc which can help in the energy sharing between two sources due to partial shading on one side of the PV panels which is discussed in next section.

The additional advantage of bidirectional switches S5, S15 is to continue the operation of the inverter as five levels in case of switch or source failure, which is discussed in detail at the later part of this section. From the proposed converter, it can be observed that the maximum voltage rating of the switching devices S1–S5, S11-S15 is Vdc, and for S6, S16, S7 and S17 is 2Vdc.

Table-1 Switching combination for Nine-level operation

Voltage levels	S1	S2	S3	S4	S5	S6	S7	S11	S12	S13	S14	S15	S16	S17
4Vdc	1	1	0	0	0	0	1	1	1	0	0	0	0	1
3Vdc	0	1	1	0	0	0	1	1	1	0	0	0	0	1
2 Vdc	0	1	1	0	1	0	0	0	1	1	0	0	0	1
Vdc	0	1	1	0	1	0	0	0	1	1	0	0	0	1
	0	1	1	0	1	0	0	0	1	1	0	1	0	0
0	0	0	1	1	0	0	1	0	1	1	0	1	0	0
	1	1	0	0	0	1	0	0	1	1	0	1	0	0
- Vdc	0	1	1	0	1	0	0	0	1	1	0	0	1	0
-2 Vdc	0	1	1	0	1	0	0	0	0	1	1	0	1	0
-3 Vdc	0	1	1	0	0	1	0	0	0	1	1	0	1	0
-4 Vdc	0	0	1	1	0	1	0	0	0	1	1	0	1	0

III. FAULT ANALYSIS OF THE NINE-LEVEL INVERTER

Generally, inverter failures are mainly due to semiconductor switch, source, and driver circuit failures. In the proposed nine-level inverter, fault tolerance is done by considering any one of the source short- or open-circuit fault and/or switch open-circuit fault. The possible switching combination for failure of the source and/or switch is given in Table-2. In case of failure (source or switch), remaining source will be active, and the total power supplied by the sources. Therefore, to avoid the overloading on the inverter, load management is suggested. During fault, the topology will be operated as a Five-level inverter, and the output voltage is maintained at rated value by using the centertap transformer at the load side. Whenever fault occurs, the control signal will be given to relays such that the primary turns of the transformer reduce to half and maintain the volt/turn ratio constant, which results to rated voltage at the secondary side of the transformer. In some of the applications, electronic gadgets and LEDs have the capability to operate at a wide range of voltage variations, i.e., at below half of the rated voltage, which avoids the use of the centertap transformer at the secondary side.

TABLE-2 Switching combination to produce Five-level voltage waveform

Voltage levels	S1	S2	S3	S4	S5	S6	S7	S11	S12	S13	S14	S15	S16	S17
+2Vdc	1	1	0	0	1	0	0	1	1	0	0	1	0	0
+Vdc	1	1	0	0	1	0	0	1	1	0	0	0	1	0
0	0	1	1	0	0	0	0	0	1	1	0	0	0	0
-Vdc	0	0	1	0	0	1	0	1	1	0	0	0	1	0
-2Vdc	0	0	1	0	0	1	0	0	0	1	0	0	1	0

In case of conventional multilevel inverter like diode clamped and flying capacitor inverter configuration, if any switch or source fail it is not possible to operate the inverter. But in case of proposed nine-level inverter configuration, it is possible to operate the inverter as a five-level inverter during the failure of switch or dc source. Possible switching combinations to produce five-level voltage shown in table.

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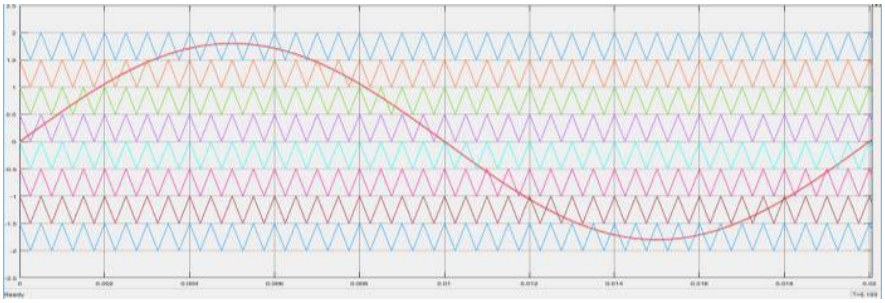

Fig2. References and Carrier waves are used for Nine-level fault tolerant inverter

Table-3 PARAMETERS FOR THE SIMULATION

Rated battery voltage	Vdc1=Vdc2=Vdc3=Vdc4=96V
Rated output voltage	240V
Modelling wave frequency	$f_m = 50Hz$
Switching frequency	$f_s = 2kHz$
Modulation index	$m_a = 0.9$
Load values	R =78 Ω, L = 50mH

IV. SIMULATION RESULTS

The Nine-level output voltage waveforms across the load and current through the load are shown in Fig. 3 for a modulation index of 0.9. Fig. 3 clearly shows nine voltage levels and nearly sinusoidal load current waveform. In Fig. 5, after 0.15 s, the fault is created, and the voltage transition from nine level to five level is shown and also demonstrates that the voltage and current magnitudes are reduced.

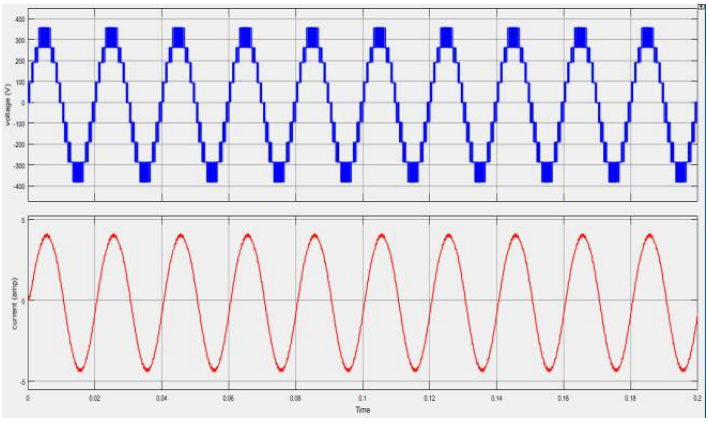

Fig 3.Top trace is the load voltage and bottom trace is load current of a nine-level inverter.

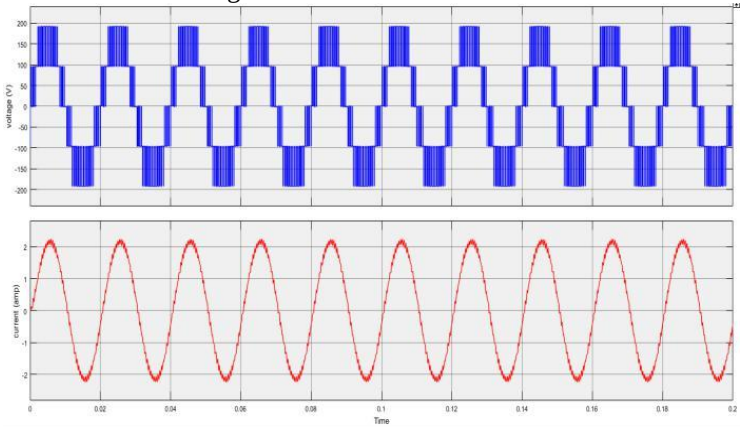

Fig 4. Top trace is the load voltage and bottom trace is load current of a five-level inverter.

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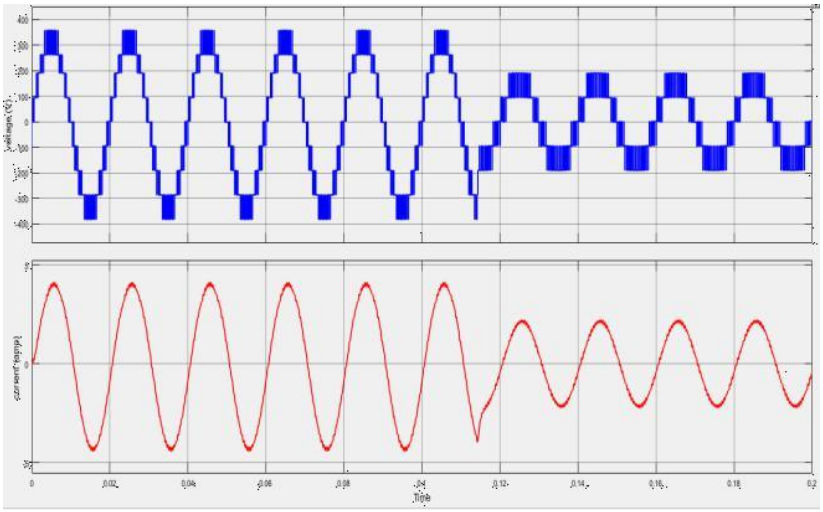

Fig 5. Top trace is the load voltage and bottom trace is load current of a nine-level inverter when change the operation from 9-level to 5-level

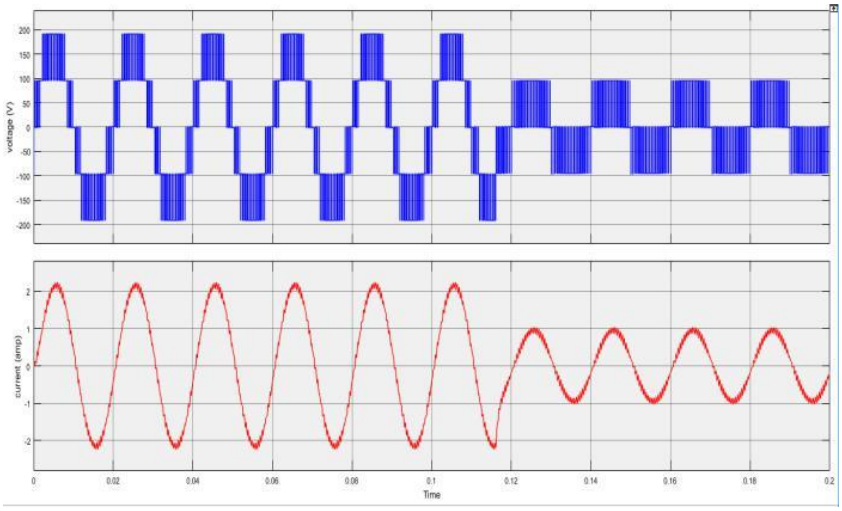

Fig 6. Top trace is the load voltage and bottom trace is load current of a five-level inverter when change the operation from 5-level to 3-leve

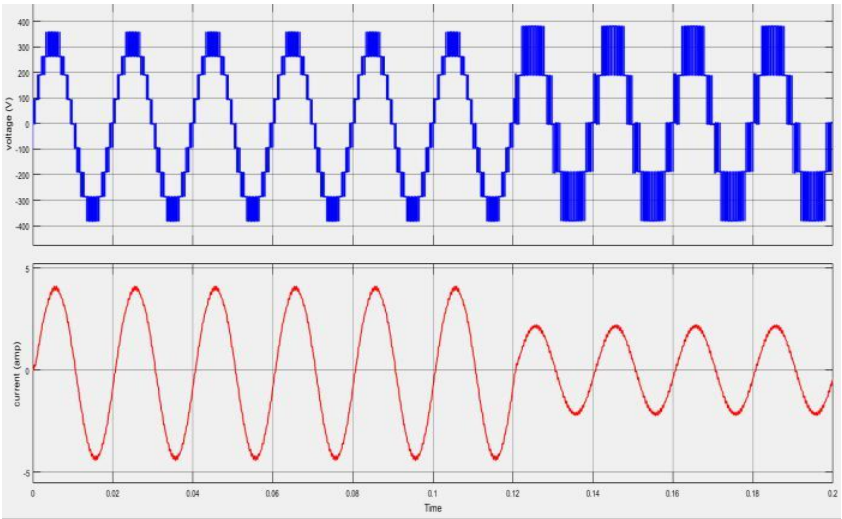

Fig 7. Top trace is the load voltage and bottom trace is load current of a nine-level inverter when change the operation from 9-level to 5-level with 1:2 Transformer for RL load.

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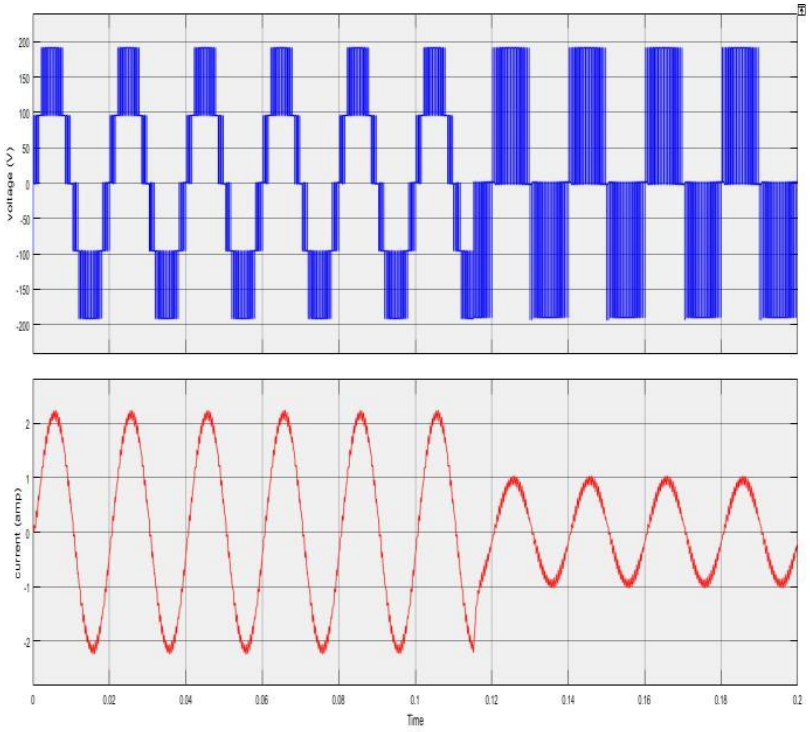

Fig 8. Top trace is the load voltage and bottom trace is load current of a nine-level inverter when change the operation from 5-level to 3-level with 1:2 Transformer for RL load.

The rated output voltage of the inverter is maintained by using a primary centertap single-phase transformer, and the corresponding waveforms are observed in Fig. 7. From Fig.5, after 0.17 s, the fault is created, and the conversion of the voltage waveform from nine-level to Five-level with the same magnitude can be observed. From Fig. 5, it can be observed that the magnitude of the current waveform is reduced by suggesting proper load management to avoid overloading on the inverter. At the time of fault, the primary turns of the transformer become half and maintain the volt/turn ratio constant, which results to rated voltage at the secondary side of the transformer.

V. CONCLUION

A novel fault tolerant Nine-level inverter configuration is proposed in this paper. The fault tolerant capability of the proposed inverter circuit is discussed in this paper. The same inverter can be operated as Five-level inverter during the failure of switching devices (or) Source. Whereas conventional neutral point clamped inverter/flying capacitor inverter cannot be operated during failure of any one switching devices. Results were presented to show the performance of the inverter both in healthy condition and different fault condition using MATLAB/Simulink. Compared to fault-tolerant five-level inverter THD is reduced using fault-tolerant Nine-level inverter.

REFERENCES

[1] A. J. Morrison, "Global demand projections for renewable energy re-sources," in *Proc. Canada EPC*, Oct. 2007, pp. 537–542.
[2] J. P. Benner and L. Kazmerski, "Photovoltaics gaining greater visibility," *IEEE Spectr.*, vol. 36, no. 9, pp. 34–42, Sep. 1999.
[3] Y. Zhao *et al.*, "Single-phase high step-up converter with improved multi-plier cell suitable for half-bridge-based PV inverter system," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2807–2816, Jun. 2014.
[4] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy re-sources," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp . 2386–2392, Sep. 2011.
[5] Y. Zhou, W. Huang, P. Zhao, and J. Zhao, "Coupled-inductor single-stage boost inverter for grid-connected photovoltaic system," *IET Power Electron.*, vol. 7, no. 2, pp. 259–270, Feb. 2014. pp.1102–1111, Apr. 2011.
[6] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[7] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
[8] E. Esfandiari and N. B. Mariun, "Experimental results of 47-level switch-ladder multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4960–4967, Nov. 2013.
[10] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched dc sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014.

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 9, September 2017

[11] S. Figarado *et al.*, "Five-level inverter scheme for an open-end winding induction machine with less number of switches," *IET Power Electron.*, vol. 3, no. 4, pp. 637–647, Jul. 2010.
[12] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel in-verter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922–929, Feb. 2015.
[13] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010
[14] I. N. S. Kumara, W. G. Ariastina, I. W. Sukerayasa, and I. A. D. Giriantari, "1 MWp grid connected PV systems in the village of Kayubihi Bali; review on location's characteristics and its technical specifications," in *Proc. ICITEE*, Oct. 2013, pp. 306 –311.
[15] A. Chen, L. Hu, L. Chen, Y. Deng, and X. He, "A multilevel con-verter topology with fault-tolerant ability," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 405–415, Mar. 2005.
[16] M. T. Dat, T. Wijnhoven, and J. Driesen, "Fault-tolerant topology of a grid-connected PV inverter coupled by a Scott transformer," in *Proc. IPEC*, Dec. 2012, pp. 428– 433.
[17] P. Lezana *et al.*, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207–2218, Jul. 2010.
[18] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase volt-age source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp 5192–5202, Oct. 2014.

BIOGRAPHIES

P. Venkatachalam received his B. Tech degree in Electrical and Electronics Engineering from Vikrama Simhapuri University, Nellore in 2014. He is currently PG scholar in JNTU Pulivendula.

K. Dileep Kumar Reddy received his B. Tech degree in Electrical and Electronics Engineering from JNTU, Hyderabad in 2011, his M. Tech degree in Electrical Power System from JNTU University, Pulivendula in 2014.